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Analysis and Design of On-sensor ECG Processors for Realtime Detection of Cardiac Anomalies Including VF, VT, and PVC

Hong-Hui Chen · Cheng-Yi Chiang · Tung-Chien Chen · Chien-Sheng Liu · Yu-Jie Huang · Shey-Shi Lu · Chii-Wann Lin · Liang-Gee Chen

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Abstract Cardiovascular disease remains the main cause of death, and great efforts are spent on the design of ECG (electrocardiogram) body sensors these years. Essential components such as analog frontend and wireless transceivers have been integrated on a compact IC with micro-Watt power consumption. To provide timely warning against the fatal vascular signs, based on the Chaotic Phase Space Differential (CPSD) algorithm, heterogeneous VLSI processors are implemented and integrated to extract the abnormal ECG characteristics for VF (Ventricular Fibrillation), VT (Ventricular Tachycardia) and PVC (Premature Ventricular Contraction). The on-sensor processing reduces 98.0% power of wireless data transmission for raw ECG signals. The application specific processor is designed to accelerate CPSD algorithm with 1.7μW power while the OpenRISC is integrated to provide the system flexibility. The architecture is realized on the FPGA platform to demonstrate the detection of the abnormal ECG signals in realtime.

Keywords Biomedical · Cardiovascular · ECG · VF · VT · PVC · CPSD

H.-H. Chen (✉) · C.-Y. Chiang · T.-C. Chen · Y.-J. Huang · S.-S. Lu · L.-G. Chen
Graduate Institute of Electronics Engineering, National Taiwan University,
Taipei, Taiwan
e-mail: sernc11@gmail.com

C.-S. Liu · C.-W. Lin
Graduate Institute of Biomedical Engineering, National Taiwan University, Taipei, Taiwan

1 Introduction

The world population is aging rapidly. It is crucial to provide adequate health care for the elders. Heart disease is one of the most prevailing and dangerous diseases among others of longevity, and remains by far the main cause of death. More than 5,000 people, for instance, experience sudden cardiac arrest (SCA) every week in the US. The chance for survival drops 10 percent per minute without defibrillation, and more than 95% of SCA victim die [1]. Thus it is of great interest to provide timely warning against fatal vascular signs.

Healthcare services are rapidly evolving from provider-centric to people-centric, with novel technologies to fulfill the demands of personalized, preventive and home-care services [2]. The goal is to develop a better mechanism that accounts for individual differences and satisfies personal needs. The signal processing algorithms on physiological signals can yield an easy-to-use realtime index of health status as well as necessary information to support decision-making in healthcare.

The research field has been an active field of research in biomedical engineering for many decades. It provides a functional assessment of a target physiological system by evaluating acquired biological signals in either the time or the frequency domain for diagnosis or treatment.

Efforts are spent on body sensors these years to support the need in the healthcare applications [3]. To build a practical realtime heart status monitoring and analyzing system, several design requirements should be considered. Compact form factor and low power consumption are two primary issues for the mobile or wearable devices.

In addition, to provide timely warning against the SCA, the system demands essential computation capability to perform signal processing algorithms in realtime. Flexibility should also be provided to adjust the algorithm parameters for different individuals and circumstances, which may easily disrupt the system robustness otherwise. Most commercial ECG holters utilize off-the-shelf components and have the lifetime less than 12 hours [4].

Early researches focus on the design optimization on individual components, and mainly discussing the analog front end design that acquires signals from human body [5–15]. However, after the signal has been acquired, it needs to be transferred to another host machine where the computation task is invoked. This requires extra power consumption. This extra penalty becomes significant especially when a wireless link is adopted to complete the transmission task.

Some other works [16–19] try to alleviate this problem by applying compression on the acquired signals. However, to deal with the SCA monitoring task, the compression scheme introduces extra delay before the SCA situation is detected. This is quite the contrary that this vital SCA situation should be discovered as soon as it happens.

Due to the advance in silicon technology, recently more components are being integrated on chip to reduce the form factor, power consumption and enabling the monitoring the vital situation in realtime. For example, a wireless transceiver and programmable digital controllers were further integrated as a system on chip (SoC) for the complete sensor node [20]. Such encapsulated sensor node could be realized in the form of a thin and flexible patch, and is capable of transmitting ECG signals wirelessly for days.

Afterwards, more digital features were explored on chip for more functionalities. For further reducing the system power some research try to achieve this goal where a sub-threshold general purpose processor (GPP) was embedded on the sensor node, and the heart rate calculation was demonstrated with 2.6 μW power [21].

Wong et al. [20] and Jocke et al. [21] tends to be generic SoCs which are not tailored for any specific application especially when it comes to the implementation of the digital parts. Our work is tailored for heart condition monitoring. Better computation efficiency could be achieved from the power consumption point of view which is explained in later sections.

In this work, a flexible architecture is proposed to deal with the difficulties of the realtime monitoring of biomedical signal related to vital physiological situation and to overcome all the above mentioned shortcomings. On-chip digital system is implemented to distinguish the normal ECG rhythm from the VF (Ventricular Fibrillation) as well as the PVC (Premature Ventricular Contraction) in realtime. Patients with PVC are at higher risk for future heart attacks as well as other cardiovascular diseases. VF may cause sudden cardiac death. The proposed system can not only record a cardiac healthy reference but also make an alarm during the SCA. The remainder of this article is organized as follows. Section 2 briefly reviews our algorithm that is previously developed and tested with human ECG data in [22]. In Section 3, the platform system utilizing HW/SW co-design with both GPP and ASP is introduced to achieve the optimized performance in terms of power efficiency and flexibility. The FPGA demonstration as well as the chip implementation result is shown in Section 4 where the characteristics of the fabricated 90 nm chip are also given. Finally, the conclusion is given.

2 Chaotic Phase Space Differential Algorithm

In most cases, the mechanism of SCA onset is a Ventricular Tachycardia (VT) that rapidly progresses to VF [23]. The Chaotic Phase Space Differential (CPSD) algorithm [22] has been developed to continuously detect critical cardiac conditions (i.e. VF, VT) based on the time-delayed phase space reconstruction method. Further, the CPSD algorithm can also distinguish other abnormal cardiovascular sign such as PVC according to the extracted feature from the ECG signal.

Figure 1a–g shows the illustration of CPSD algorithm. In training mode, the algorithm finds a steady ECG window of length W seconds as the reference. And in testing mode, it compares the current signal with the reference to obtain the index of variation. The signal $s(t)$ in the window

$$W(t_{\text{current}}) = \{t_i \mid t \in [t_{\text{current}} - W + d, t_{\text{current}}]\} \tag{1}$$

where d is the time delay used to form phase space vector, is plotted in a diagram according to the following steps.

(1) Construct the phase vectors
The phase space vector v is obtained by the delayed signal pairs.

$$v(t_i) = \langle s(t_i - d), s(t_i)\rangle, t_i \in W(t_{\text{current}}) \tag{2}$$

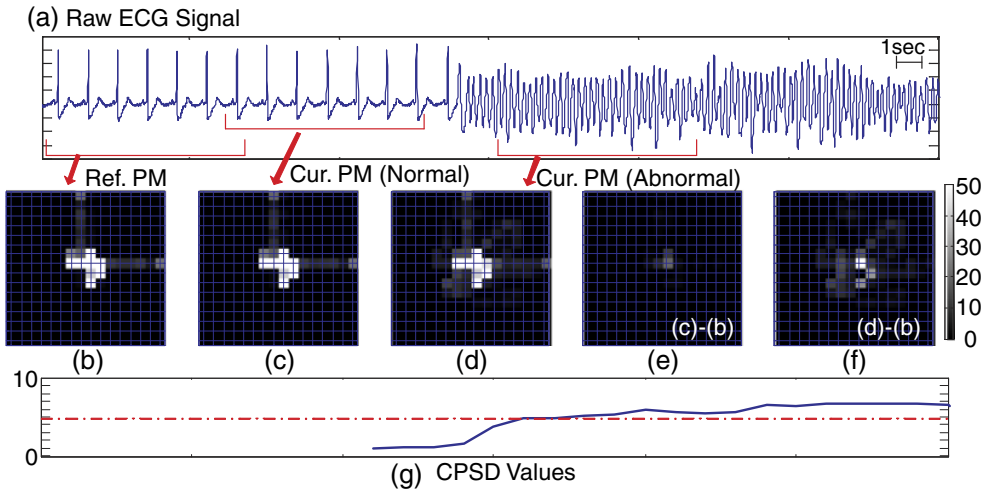

Figure 1 The illustration of CPSD algorithm. **a** is the ECG signal derived from normal into VF. **b** is the phase space matrix constructed from normal ECG signal in the training state and served as a reference in the testing stage. **c** is the phase space matrix constructed from normal ECG signal in testing, while **d** is the phase space matrix constructed from VF ECG signal in testing. **e** and **f** shows the difference phase space matrix of **b**–**c** and **d**–**c**, respectively. A typical VF ECG signal spreads out on the phase space while normal ECG signal does not. **g** shows the corresponding CPSD value and threshold for VF.

(2) Quantize the phase vector
Quantize each dimension of the vector into L levels based on M to get $v^*(t_i)$.

$$v^*(t_i) = \left\langle \left\lfloor \frac{(s(t_i - d) + M)L + M}{2M} \right\rfloor, \left\lfloor \frac{(s(t_i) + M)L + M}{2M} \right\rfloor \right\rangle, \quad (3)$$

$$t_i \in W(t_{\text{current}})$$

where $M = max(|s(t_i)|), t_i \in W(t_{\text{reference}})$ is the maximum absolute value in the reference window. Note that signal in current window is saturated into $[-M, M]$ after a valid reference has been found.

(3) Construct the phase space matrix (PSM)
A two-dimensional PSM, S_M, can be constructed from the normalized ECG signal segment, $v^*(n)$, with delay index, d. The number of visited-times on the S_M with coordinate of $(v^*(n), v^*(n + d))$ is counted by Eq. 4 from 0 to $N - d$ where N is the total number of samples in window W.

$$S_M[v^*(n_x), v^*(n_x + d)] = S_M[v^*(n_x), v^*(n_x + d)] + 1, \quad \text{for } n_x = 0 \text{ to } N - d \quad (4)$$

where $S_M[\ ]$ represents the intensity matrix of accumulated visited number on the S_M. Following the presentation of the basic method for constructing PSM, the constructed reference template, Reference Phase Space Matrix (RPSM), the experimental segments, and Experimental Phase Space Matrix (EPSM) are used to calculate the CPSD value in later section.

(4) Compute the difference phase space matrix
Because the CPSD algorithm focuses on the spatial-temporal changes of PSM, we use the absolute values of the differential matrix, DPSM, between EPSM and RPSM to calculate the complexity value (CV) according to Eqs. 5 and 6. The complexity value (CV) of DPSM is defined as the number of all array elements that exceed zero.

$$S_{\text{DPSM}}[x, y] = |S_{\text{EPSM}}[x, y] - S_{\text{RPSM}}[x, y]|, \quad \text{for } x, y = 0 \text{ to } N \quad (5)$$

$$CV = \left\{ \begin{matrix} CV + 1, S_{\text{DPSM}}[x, y]! = 0 \\ CV, \text{otherwise} \end{matrix} \right\}, \quad \text{for } x, y = 0 \text{ to } N \quad (6)$$

(5) Compute the CPSD value
The first CV of each ECG segment is adopted as a normalization factor in determining the subsequent CV to obtain the final CPSD values, as calculated by Eq. 7, which minimize the possible intra- and inter-patient variations. Self-

normalization of each individual's normal ECG patterns enables the establishment of a normal range of baseline CPSD values.

$$CPSDn = \frac{CV_n}{CV_1}, \text{ where } n \geq 1 \tag{7}$$

In the above steps, the algorithm requires a reference phase space matrix that is suitable for each individual. The algorithm adaptively generates a reference phase space matrix during each trial instead of deriving it from databases. In the training stage, a candidate phase space matrix corresponding to signal in $W(t_{\text{candidate}})$ is constructed, and is then compared to a checking phase space matrix corresponding to signal in $W(t_{\text{candidate}+1})$. If the difference satisfies

$$Diff(PSM_{\text{candidate}+1}, PSM_{\text{candidate}}) < Threshold_{\text{valid}}\ h \tag{8}$$

the candidate phase space matrix becomes a valid reference phase matrix, and remains its value throughout testing stage. If the candidate fails the test, the signal in the next window would serve as the candidate. The reference is updated in a period of 30 s to track the variation of the reference signal. Generally, the training stage takes 8–9 s upon started for finding a proper reference PSM. The reference signal collected and validated in realtime makes the algorithm adapted to each individual during each trial.

A simplified example is given according to the above mentioned procedures. Assume an input sequence after digitized by ADC is given as follows:

S_{in} = [9 16 28 33 25 17 10 19 26 35 27 16 9 18 24 32 25 18 8 23]

If the time delay parameter d is assigned as, for example, 5, the space vectors are generated as follows:

$v0 = (9, 17)$; $v1 = (16, 10)$; $v2 = (28, 19)$;

$v3 = (33, 26)$; $v4 = (25, 35)$; $v5 = (17, 27)$;

$v6 = (10, 16)$; $v7 = (19, 9)$; $v8 = (26, 18)$;

$v9 = (35, 24)$; $v10 = (27, 32)$; $v11 = (16, 25)$;

$v12 = (9, 18)$; $v13 = (18, 8)$; $v14 = (24, 23)$;

M equals to 35 which is the maximum absolute value of vector Sin. Select quantized level $L = 6$, space vectors are quantized as:

$v0_q = (4, 4)$; $v1_q = (4, 4)$; $v2_q = (5, 5)$;

$v3_q = (6, 5)$; $v4_q = (5, 6)$; $v5_q = (4, 5)$;

$v6_q = (4, 4)$; $v7_q = (5, 4)$; $v8_q = (5, 5)$;

$v9_q = (6, 5)$; $v10_q = (5, 6)$; $v11_q = (4, 5)$;

$v12_q = (4, 5)$; $v13_q = (5, 4)$; $v14_q = (5, 5)$;

The quantized vectors are the elements of phase space matrix. Plot of the occurrence count of quantized vectors in matrix could be illustrated in Fig. 2b. If RPSM and EPSM are got as Fig. 2a and b, the difference of the two matrix will be Fig. 2c. The resulting DPSM contains zero and non-zero terms. CV value is calculated as follows:

$CV = 6$ (*non − zero term numb er in* Fig. 2c)

A reference DPSM value is selected according to Eq. 8 as CV_1. Assuming here the CV_1 from reference DPSM is 2, the final CPSD value is calculated as follows:

$$CPSD_n = \frac{CV_n}{CV_1} = \frac{6}{2} = 3$$

If CPSD value is generated, the live status of heart could be judged. The thorough algorithm flow is depicted as Fig. 3. Threshold TH1 and TH2 is defined based on the evaluation result from more than 4 thousand cases from several ECG signal databases [24–28] for detecting AF/VF situations.

Figure 1a–g shows an typical VF signal and the corresponding CPSD value. To distinguish different cardiovascular diseases from the CPSD value, a set of thresholds along with other parameters were optimized and described in [22]. According to [22], the statistical results of PVC, VF/VT from MIT arrhythmia databases [29] showed that the CPSD algorithm successfully identified PVC, VF/VT with sensitivity and specificity greater than 95%. Besides detecting fatal

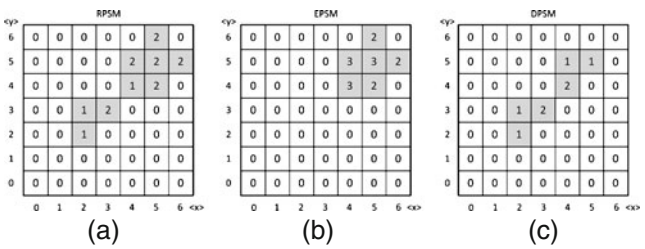

Figure 2 RPSM, EPSM and corresponding DPSM.

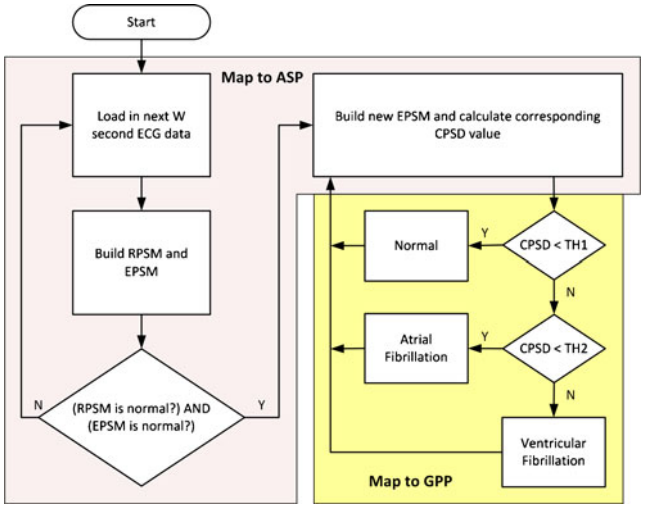

Figure 3 Realtime heart status monitoring flow.

signs, the CPSD value can also serves as an index of interest in the further processing of ECG signal such as compression, storage, transmission, and other detailed analysis. Hence, it is an algorithm suitable for heart status monitoring system.

There are several parameters in the CPSD algorithm, such as window length W, matrix size N, constant time delay d between two dimensions in the phase vectors etc. In practice, it is of great merit to retain flexibility in the system. For example, the threshold of difference h between reference matrix and current matrix should be larger in the presence of large background noise.

The performance of the existing algorithm is well studied in [4]. Comparison with the existing algorithms reveals that CPSD's VF classification performance is only slightly worse than that of GDA + SVM [30], but the proposed method has benefit of low-cost implementation for real-time application. This algorithm is also the best for all cited algorithms in AF analysis.

3 Proposed On-sensor ECG Processors

Design requirements for our system come from many aspects. First, our system should be flexible to support as many medical applications as possible. Besides, the system should fulfill the need for practical usage. In case of mobile medical devices the power consumption should be kept as low as possible in order to extend the lifetime of the device. Finally computation capability should be sufficient in order to response the detected abnormal situation in realtime.

3.1 Platform-based Biomedical System

Most of the modern SoC design projects adopt platform based architecture for flexible hardware and software integration. As for the medical industrial, systems implemented with discrete components are the main stream strategy for the current participating vendors. For fulfilling better health care requirements, more functions tend to be incorporated into a single device. For example, a device could measure blood pressure, heart rate, pulse oximetry, and ECG. Our current research focuses on using ECG to detect heart disease and platform based implementation is selected with an eye to extend our system in the future for dealing with other biomedical signals.

There is another potential advantage of designing a SoC. The U.S. FDA requires the components used for fabricating medical devices to be available for at least 5 years [31] in market. SoC design could reduce the external component counts and this makes it easy to acquire the FDA approval.

3.2 Heterogeneous Processors

Figure 4 shows the architecture of the proposed system. The ECG signals are amplified and digitized by the analog recording interface circuit, and then input to the digital section sample by sample. The digital section has two processors. The CPSD processor is an application specific processor (ASP) extracting the CPSD values on-line from the raw ECG samples. Afterwards, the OpenRISC, a 32-bit general purpose processor (GPP), is used to decide if there is a fatal sign or not based on the extracted CPSD values. User interfaces such as the wireless transceiver and an I^2C port are connected via the wishbone system bus and are controlled by the GPP.

Two levels of power reduction are achieved with this system hierarchy. First, in the traditional design, the sensor node transmits the raw ECG signals to the base node where the processing is generally performed.

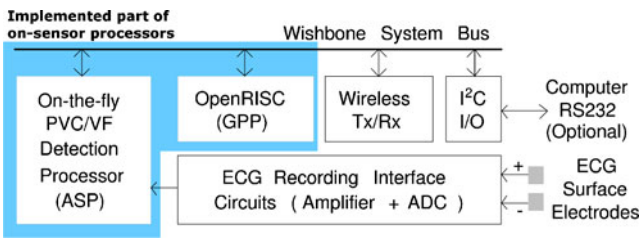

Figure 4 The architecture of the proposed system with the on-chip ASP and GPP.

However, transmitting the raw ECG signals wirelessly consumes a significant power in this case. We move the computing load from the base node to the sensor, and trade the transmission power with the computation power through the on-chip signal processing. After the signal processing, the raw data could be sent only if a fatal ECG sign is detected. The transmitter can stay asleep or send only the extracted features in the normal situation.

The second level of power reduction focuses on the on-chip signal processing. The processing on raw ECG signals such as filtering, vector extraction, and matrix operation has great requirement on data accessing. Utilizing the GPP for these operations requires continuous data fetching and storing between SRAMs and registers, and is less efficient in power consumption. We utilize both the ASP and GPP in our system to reflect the need of the application. To improve the power efficiency, the ASP is designed to accelerate the CPSD algorithm with the customized memory hierarchy and parallel processing units. The GPP can thus be operated with a much lower operation frequency and provide the flexibility for the system. Besides the final result of the CPSD value, the GPP can also be programmed to decide the response after the detection of the fatal ECG sign. The algorithm and hardware parameters such as the threshold value and the gain of the amplifier can also be adjusted by GPP if required.

3.3 Application Specific Processor for CPSD

Figure 5 shows the architecture of CPSD ASP. The inputs are the 10-bit bit-parallel sample-serial ECG samples from the ADC. The outputs are the CPSD values. The CPSD is generated once per second and can be retrieved by GPP through the interrupt interaction. The ASP has four processing pipelines, and the ECG samples keep streaming through the pipeline buffers for CPSD operations. This customized structure avoids the redundant data fetching and results in the low power consumption.

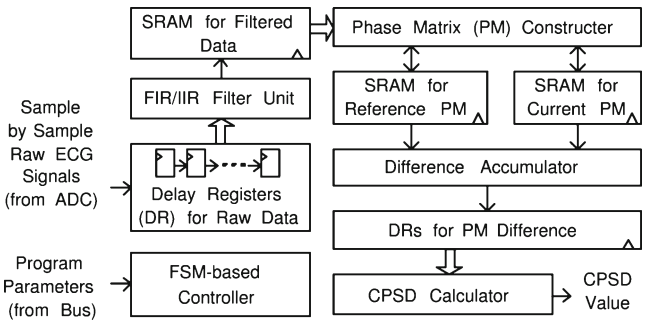

Figure 5 The block diagram of the integrated ASP for CPSD acceleration.

A filter unit is placed in the first pipeline to remove the artifacts such as the low-frequency drifting voltage and the 60 Hz power line noise. The filter is designed with cascaded multiply-accumulate (MAC) units, and the filter coefficients are able to be programmed through the system bus. One SRAM is used to store an 8-second window of the filtered ECG samples after the filtering. In the second pipeline, the Phase Matrix Constructer scans through the SRAM of the filtered data, extracts the phase vectors, and then constructs the corresponding phase space matrix in the PM SRAMs. The third pipeline compares two PMs in the PM SRAMs and accumulates the differences. The last pipeline calculates the CPSD value with the latest PM differences according to Eqs. 6 and 7.

The ASP has two operation phases—the training phase and on-line processing phase. After the system reset, the training phase finds the reference PM according to Eq. 8. The reference PM stands for the normal ECG pattern specific for each user. After the training, the ASP enters the online processing phase and keeps comparing the current PM with the reference one. Note that the retraining can be activated to adapt the change of the environment by the GPP if required.

4 Implementation Results

4.1 FPGA Demonstration

The proposed digital system is implemented with Verilog language and is physically demonstrated with FPGA platform (Xilinx ML505 with XC5VLX110T FPGA) as shown in Fig. 6. The ECG signals are first amplified and filtered by the in-house instrument amplifier IC. Then the A/D converter on FPGA board converts the analog ECG into digital samples at 256 samples per second (sps). Afterwards, the digital samples are input to the proposed digital system with ASP and GPP for the CPSD calculation. The filter coefficients programmed in ASP are designed to support a 1–100 Hz band pass filter and two notch filters around 60 Hz and 120 Hz. The programming is done through the RS-232 in this demonstration. The CPSD value is computed by the ASP while thresholding of the CPSD value is performed by the GPP. 11.7% of the logic slices and 19.6% of the distributed SRAM bits are consumed according to the report of implementation result. The FPGA is connected to a laptop with USB to RS-232 cable, and the filtered raw data as well as the CPSD index are fetched and displayed with GUI

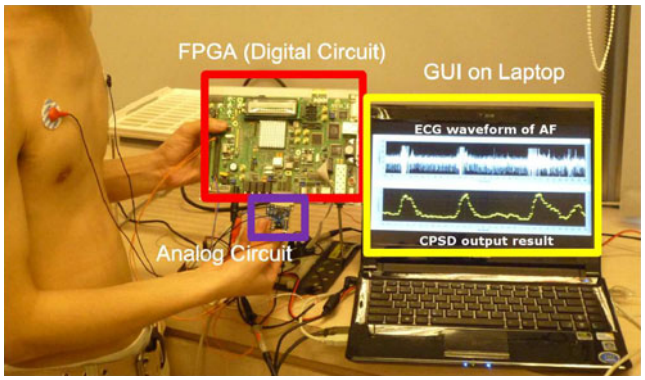

Figure 6 The ECG signals are amplified and filtered by the in-house instrument amplifier IC. Then the A/D converter on FPGA board converts the analog ECG into digital samples at 256 samples per second (sps). Afterwards, the proposed digital system with ASP and GPP performs the CPSD calculation. The FPGA is connected to a laptop with RS-232, and the filtered raw data as well as the CPSD index are fetched and displayed with GUI on the screen.

on the screen. The GUI software on PC host is developed with QT 4. It involves two threads. The first one continuously polls the ready status of new CPSD computation result. Once ready the result is pulled back to PC. The other thread draws the CPSD value on the widget provided by QT where a curve of CPSD history is shown on the screen for inspection.

4.2 Synthesis Result and Comparison

Proposed design is synthesized in 90 nm low-leakage CMOS process. Table 1 summarizes the implementation results. The power consumption between different systems of the sensor node is compared in Table 2. The power of amplifier and ADC refers to [21] while the power of wireless transmission unit refers to [20]. The power is scaled to fit the scenario of sampling resolution at 10 bit and 256 sps. Since the transmitter can be turned off dynamically by the GPP, we assume the wireless Tx power is in proportional to the transmission data rate. According to the GNU GCC compiler

Table 1 Implementation results of digital section in 90 nm CMOS process.

Process	90 nm 1P9M Low Leakage CMOS	
supply voltage	1.0 Volt	
	CPSD ASP	OpenRISC GPP
Gate count	18050	32214
SRAM bits	25600	196608
Operation frequency	100 KHz	4 KHz
Power consumption	1.704μW	3.823μW
(Dynamic/leakage)	(1.437/0.267)	(0.103/3.720)

Table 2 Power analysis of different architectures.

	No processing	GPP only	ASP only	Proposed
Amplifier[21]	1.55	1.55	1.55	1.55
ADC[21]	0.41	0.41	0.41	0.41
GPP	–	423.11	–	3.82
ASP	–	–	1.70	1.70
Wireless Tx[20]	107.11	0.67	0.67	0.67
Total	109.07	425.74	4.33	8.16

(Unit: μW)

of the OpenRISC, 4 MIPS computation complexity is required if the whole CPSD algorithm is performed by the GPP in realtime. 0.423 mW power consumption is thus required according to the synthesized results.

In the case of no processing on chip, the sensor node continuously sends the raw ECG samples to the base node, and the processing is done on the base node. In this case, 98% of power consumption is consumed by the wireless Tx unit on the sensor node. The power consumption of wireless transmission can be reduced using on-chip processing. However, if only the GPP is integrated, because of its poor power efficiency for the data stream processing, a larger power of 425.7μW is required, which conflicts the main purpose of the design. If the whole algorithm is implemented with an ASP, the power consumption is significantly reduced by 98.9% as shown in the third column. However, this architecture lacks the flexibility and may violate the application requirements.

In the proposed architecture with both ASP and GPP, because the main routine is performed by the ASP, the GPP can work with a lower operation frequency, and provide the essential flexibility with only 3.82μW power.

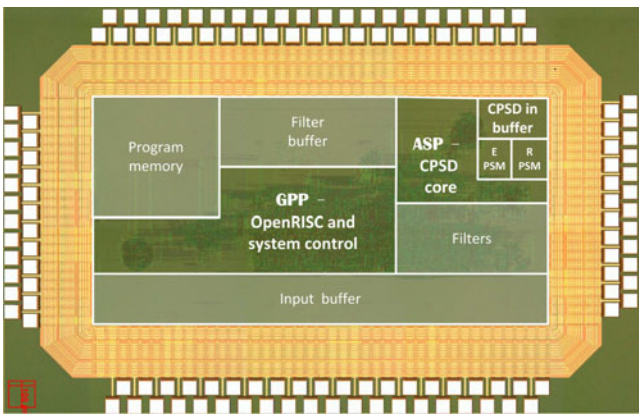

Figure 7 90 nm digital part chip photo.

Table 3 Fabricated chip profile.

Technology	9 0nm 1P9M LL
Supply voltage	1.0 Volt
Operation frequency	GPP: 100 KHz ASP: 4 KHz
Area	$2780\times1782\ \mu m^2$
Power	$5.8\ \mu W$

4.3 Real Chip profile

The proposed ASP + GPP architecture is fabricated in UMC 90 nm technology. The chip photo is shown in Fig. 7. The profile of the fabricated chip is listed in Table 3. Measurement is done on tester machine, Agilent 93000, and chip's functions are basically working by applying short-term test patterns. More complete system test will be conducted after the chip has integrated with our existing in-house analog chip to the same board. The measured power consumption is 5.8 μW for the GPP and ASP modules.

5 Conclusion

In this paper, on-sensor ECG processors are designed for the realtime heart monitoring and analyzing SoC to give a timely warning against the fatal vascular signs. The system consists of an ASP to accelerate the CPSD algorithm as well as a GPP to control the system and provide better flexibility. Different architectures are discussed and compared, which leads to the conclusion that processing on the sensor node can reduce 98% power of wireless transmission for the raw ECG signals. Also the ASP can be used to incorporate with GPP and reduce the power consumption of the GPP by 99%. Such HW/SW co-design is a trade-off between processing efficiency and flexibility, and the proposed system achieves an optimized balance through the careful analysis.

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Cheng-Yi Chiang was born in Taipei, Taiwan, in 1986. He received the B.S., and M.S.degrees in electrical engineering from National Taiwan University, Taipei, Taiwan in 2008, and 2011. His current research interests are signal processing of electrocardiography and electroencephalography. He is currently working for the algorithm and architecture design for smart biomedical sensors and closed-loop neuroprosthetic devices.

Hong-Hui Chen was born in Taipei, Taiwan, in 1978. He received the B.S., M.S. degrees in electrical engineering from National Taiwan University, Taipei, Taiwan in 2000, 2002. Currently he is working toward the Ph.D. degree in electronic engineering at National Taiwan University, Taipei, Taiwan. His research interests include algorithm developments, system level analysis/design/integration and system-on-a-chip (SoC) realization for bio-medical applications.

Tung-Chien Chen was born in Taipei, Taiwan, in 1979. He received the B.S., M.S., and Ph.D. degrees in electrical engineering from National Taiwan University, Taipei, Taiwan in 2002, 2004, and 2009. He was a visiting scholar in University of California, Santa Cruz, from 2006 to 2008. Before 2006, he worked on the algorithm and architecture design for multimedia applications such as video codecs and intelligent video sensors. He is currently working for the algorithm and architecture design for smart biomedical sensors and closed-loop neuroprosthetic devices.

Chien-Sheng Liu was born in Changhua, Taiwan, in 1974. He received the M.S. degree in biomedical engineering from National Yang-Ming University, Taipei, Taiwan in 2002 and the Ph.D. degree in electrical engineering from National Taiwan University, Taipei, Taiwan in 2010. Before 2011, he worked on the algorithm design for real-time analysis of ECG signal. He is currently working on the algorithm development and device design for smart biomedical sensing network application.

Shey-Shi Lu (S'89-M'97-SM'99) received the B.S. degree from National Taiwan University, Taipei, Taiwan, in 1985, the M.S. degree from Cornell University, Ithaca, NY, in 1988, , and the Ph.D. degree from the University of Minnesota at Minneapolis-St. Paul, in 1991, all in electrical engineering. During the summer of 1990, he was a Research Aide with the IBM T. J. Watson Research Center, where he was involved with diffusion ohmic contact. In August 1991, he joined the Department of Electrical Engineering, National Taiwan University, as an Associate Professor, becoming a Full Professor in 1995. His current research interests are in the areas of CMOS RFICs and CMOS biotechnology.

Dr. Lu was the recipient of the 2009 Outstanding Research Award of the National Science Council, the 2006 Distinguished Engineering Professor Award of the Chinese Institute of Electrical Engineering, and the 2005 Fu Szu-Nien Award of National Taiwan University.

Yu-Jie Huang received the B.S. degree in electrical engineering from National Cheng Kung University, Tainan, Taiwan, in 2006.He is currently working toward the Ph.D. degree in electronic engineering at National Taiwan University, Taipei, Taiwan. His research interests include CMOS mixed-signal integrated circuits design and system-on-a-chip design for wireless sensing and bio-medical application.

Chii-Wann Lin received his B.S. from Department of Electrical Engineering, National Cheng-Kung University in 1984. He then started his career in biomedical engineering with M.S. degree from Graduate Institute of Biomedical Engineering, National Yang-Ming University in 1986. He received his Ph.D. from Case Western Reserve University in 1993. He joined the Center for Biomedical Engineering, College of Medicine, National Taiwan University from Sept. 1993 till Aug. 1998. He is now a professor in Graduate Institute of Biomedical Engineering and holds joint

appointments in both Department of Electrical Engineering and Institute of Applied Mechanics, National Taiwan University. He is also a member of IEEE EMBS, IFMBE, ACST and Chinese BMES. He is the President of Taiwan Association of Chemical Sensors (ACST) from 2008–2010. His research interests include biomedical micro sensors, optical biochip, surface plasmon resonance, bio-plasmonics, nano-medicine, and personal e-health system.

Liang-Gee Chen was born in Yun-Lin, Taiwan, in 1956. He received the BS, MS, and Ph.D degrees in Electrical Engineering from National Cheng Kung University, in 1979, 1981, and 1986, respectively. He was an Instructor (1981–1986), and an Associate Professor (1986–1988) in the Department of Electrical Engineering, National Cheng Kung University. In the military service during 1987 and 1988, he was an Associate Professor in the Institute of Resource Management, Defense Management College. From 1988, he joined the Department of Electrical Engineering, National Taiwan University. During 1993 to 1994 he was Visiting Consultant of DSP Research Department, AT&T Bell Lab, Murray Hill. At 1997, he was the visiting scholar of the Department of Electrical Engineering, University, of Washington, Seattle. Currently, he is Professor of National Taiwan University. From 2004, he is also the Executive Vice President and the General Director of Electronics Research and Service Organization (ERSO) in the Industrial Technology Research Institute (ITRI). His current research interests are DSP architecture design, video processor design, and video coding system.

Dr. Chen is a Fellow of IEEE. He is also a member of the honor society Phi Tan Phi. He was the general chairman of the 7th VLSI Design CAD Symposium. He is also the general chairman of the 1999 IEEE Workshop on Signal Processing Systems: Design and Implementation. He serves as Associate Editor of IEEE Trans. on Circuits and Systems for Video Technology from June 1996 until now and the Associate Editor of IEEE Trans. on VLSI Systems from January 1999 until now. He was the Associate Editor of the Journal of Circuits, Systems, and Signal Processing from 1999 until now. He served as the Guest Editor of The Journal of VLSI Signal Processing Systems for Signal, Image, and Video Technology, November 2001. He is also the Associate Editor of the IEEE Trans. on Circuits and Systems II: Analog and Digital Signal Processing. From 2002, he is also the Associate Editor of Proceedings of the IEEE.

Dr. Chen received the Best Paper Award from ROC Computer Society in 1990 and 1994. From 1991 to 1999, he received Long-Term (Acer) Paper Awards annually. In 1992, he received the Best Paper Award of the 1992 Asia-Pacific Conference on Circuits and Systems in VLSI design track. In 1993, he received the Annual Paper Award of Chinese Engineer Society. In 1996, he received the Out-standing Research Award from NSC, and the Dragon Excellence Award for Acer. He is elected as the IEEE Circuits and Systems Distinguished Lecturer from 2001–2002.